Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.048”**

**.075”**

***LT***

**111**

**MASK**

**REF**

**FUSE**

**LINK**

**V-**

**-IN**

**BAL**

**+IN**

**BAL/STROBE**

**GND**

**OUT**

**V+**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” min.**

**Backside Potential:**

**Mask Ref: 111**

**APPROVED BY: DK DIE SIZE .048” X .075” DATE: 11/9/21**

**MFG: LINEAR TECH THICKNESS .015” P/N: LM111**

**DG 10.1.2**

#### Rev B, 7/19/02